electro-less plating layers 150 exposed through the upper openings 310 and not protected by the etch resist 410. While the conductive layers 220 are exposed to the etch, the etch rate is slow enough such that the thinner plating layer 150 is removed while the thicker conductive layer 220 remains. The etch resist 410 prevents the previously exposed plating layer 150 on the second side from being etched away, thus allowing the plating layers 150 to maintain an electrical connection across the second side of the substrate 100, and to portions of the first side through the metal interconnect 130 and via 120."

A3 Cont'd

(4) Please amend the title as follows:

A4

METHOD OF MANUFACTURING A PRINTED WIRING BOARD HAVING A DISCONTINUOUS PLATING LAYER

IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) A method of plating an electrical contact on a substrate, comprising:

A5

forming a metal interconnect on first and second opposing sides of a printed wiring board and through a via formed through the printed wiring board;

Sub B1

forming first and second dielectric layers on the metal interconnect over the first and second sides of the printed wiring board, respectively, the first and second dielectric layers each having openings therethrough that expose portions of the metal interconnect;

forming first and second plating layers on the first and second dielectric layers, respectively, and in the first and second openings and on the exposed portions of the metal interconnect, the first and second plating layers electrically connected by the metal interconnect;

electroplating first and second contact layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second dielectric layers while leaving the portions of the first and second plating layers under the first and second contact layers.

Sub B1 A5 Cont'd

(2) Please amend Claim 2 as follows:

2. (Amended) The method as recited in Claim 1 wherein forming first and second plating layers includes forming the first and second plating layers with an electro-less process and the method further includes electroplating first and second conductive layers on the first and second plating layers, respectively.

(3) Please amend Claim 3 as follows:

3. (Amended) The method as recited in Claim 1 wherein electroplating first and second contact layers includes electroplating first and second barrier layers over the first and second plating layers, respectively.

(4) Please amend Claim 4 as follows:

4. (Amended) The method as recited in Claim 3 wherein electroplating first and second barrier layers includes electroplating first and second nickel layers, respectively, and electroplating first and second contact layers further includes electroplating first and second gold layers on the first and second nickel layers, respectively.

(5) Please amend Claim 5 as follows:

5. (Amended) The method as recited in Claim 1 wherein forming the first plating layer includes forming a discontinuous first plating layer.

Sub B1

(6) Please amend Claim 6 as follows:

6. (Amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer prior to electroplating the first and second contact layers.

cont'd

(7) Please amend Claim 7 as follows:

7. (Amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer subsequent to electroplating the first and second contact layers.

(8) Please amend Claim 8 as follows:

8. (Amended) A method of manufacturing an integrated circuit (IC) substrate, comprising:

forming a multi-layered substrate with a printed wiring board core and having vias formed therethrough;

forming metal interconnects on first and second opposing sides of the printed wiring board and through the vias;

forming first and second dielectric layers on the metal interconnects over the first and second sides of the printed wiring board, respectively, the first and second dielectric layers each having openings therethrough that expose portions of the metal interconnects; and

plating an electrical contact on the substrate, including:

forming first and second plating layers on the first and second dielectric layers, respectively, and in the first and second openings and on the exposed portions of the metal interconnects, the first and second plating layers electrically connected by one of the metal interconnects;

electroplating first and second contact layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second dielectric layers while leaving the portions of the first and second plating layers under the first and second contact layers.

(9) Please amend Claim 9 as follows:

9. (Amended) The method as recited in Claim 8 wherein forming the first and second plating layers includes forming the first and second plating layers with an electro-less process and

the method further includes electroplating first and second conductive layers on the first and second plating layers, respectively.

(10) Please amend Claim 10 as follows:

10. (Amended) The method as recited in Claim 8 wherein electroplating first and second contact layers includes electroplating first and second barrier layers over the first and second plating layers, respectively.

(11) Please amend Claim 11 as follows:

11. (Amended) The method as recited in Claim 10 wherein electroplating first and second barrier layers includes electroplating first and second nickel layers and electroplating first and second contact layers further includes electroplating first and second gold layers on the first and second nickel layers.

(12) Please amend Claim 12 as follows:

12. (Amended) The method as recited in Claim 8 wherein forming the first plating layer includes forming a discontinuous first plating layer.

(13) Please amend Claim 13 as follows:

13. (Amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer prior to electroplating the first and second contact layers.

(14) Please amend Claim 14 as follows:

14. (Amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer subsequent to electroplating the first and second contact layers.

(15) Please cancel Claim 15 without prejudice or disclaimer.

(16) Pursuant to the previous election of Claims 1-15 in response to a restriction requirement, please cancel Claims 16-20 without prejudice or disclaimer.

(17) Please add new Claims 21-24 as follows:

--21. (New) The method as recited in Claim 1 wherein the first and second plating layers are not formed in the via.

22. (New) The method as recited in Claim 2 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the first and second openings, respectively.

23. (New) The method as recited in Claim 8 wherein the first and second plating layers are not formed in the vias.